Course Type	Course Code	Name of Course	L	T	P	Credit
DE	NECD549	VLSI Signal Processing	3	0	0	3

Course Objective

This course will introduce approaches and methodologies for VLSI design of signal processing.

- To introduce techniques for altering the existing DSP structures to suit VLSI implementations.
- To introduce efficient design of DSP architectures suitable for VLSI

Learning Outcomes

Upon successful completion of this course, the students will:

- Understand VLSI design methodology for signal processing systems.
- Be familiar with VLSI algorithms and architectures for DSP.
- Be able to implement basic architectures for DSP using CAD tools.

Unit No.	Topics to be Covered	Lecture Hours	Learning Outcome
1	Introduction to DSP systems – Typical DSP algorithms, Data flow and Dependence graphs – critical path, Loop bound, iteration bound, Longest path matrix algorithm,Pipelining and Parallel processing of FIR filters, Pipelining and Parallel processing for low power.	9	The students will be introduced to the basic concepts of VLSI algorithms for DSP systems along with pipelining and parallel processing architecture.
2	Retiming – definitions and properties, Unfolding – an algorithm for unfolding, properties of unfolding, sample period reduction and parallel processing application, Algorithmic strength reduction in filters and transforms	5	The students will learn the retiming concept, algorithmic strength reduction of filters.
3	2-parallel FIR filter, 2-parallel fast FIR filter, DCT architecture, rank-order filters, Odd-Even merge-sort architecture, parallel rank-order filters.	6	The students will learn the concept of FIR filters
4	Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm, Pipelined and parallel recursive filters – Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with powerof-2 decomposition	5	The students will learn thefast convolution, pipelining architecture of IIR filters.
5	Clustered look-ahead pipelining, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.	6	The students will learn the concept of parallel processing of IIR filters.
6	**Bit-level arithmetic architectures:** Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers.	5	The students will learn the bit-level arithmetic architectures.
7	Design of Lyon's bit-serial multipliers using Horner's rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner"s rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters.	6	The students will learn the concepts of bit level multiplier architecture.
	Total	**42**	

Text Book:

1. Keshab K. Parhi, "VLSI Digital Signal Processing Systems, Design and implementation ", WileyInterscience.

Reference Books:

1. U. Meyer – Baese, "Digital Signal Processing with Field Programmable Gate Arrays", Springer, Second Edition.
2. Mohammed Ismail, Terri, Fiez, Analog VLSI Signal and Information Processing, McGraw Hill.
3. Kung. S.Y., H.J. While house T.Kailath, VLSI and Modern signal processing, Prentice Hall.
4. Jose E. France, YannisTsividls, "Design of Analog Digital VLSI Circuits for Telecommunications and Signal Processing", Prentice Hall.